REMARKS

Reconsideration of the above-identified application in view of the present amendment is respectfully requested.

A certified copy of the Swiss foreign priority document as well as a corresponding English translation verified by the translator is being filed, under separate cover, to eliminate the availability of cited U.S. patent no. 6,324,328 to Mehlhorn et al. as prior art for the present application. The Swiss foreign priority document has a date of February 23, 1999 which pre-dates the U.S. filing date of June 16, 1999 of the patent to Mehlhorn et al. (See MPEP §201.15). Thus, the rejection of claims 1-3, 7, 9-10, 14-17 under 35 USC §102(e) as being anticipated by Mehlhorn et al. should be withdrawn. The rejection of claim 6 under 35 USC 103(a) as being unpatentable in view of Mehlhorn et al. should also be withdrawn.

Of the claims rejected by Mehlhorn et al., claims 3, 6 and 14 have not been rejected under any other statutory provision. Thus, claims 3, 6 and 14 should be allowable.

In the alternative, claims 1-3, 7, 9-10, 14-17 and 6 patentably define over the patent to Mehlhorn et al. Anticipation requires a single prior art reference that discloses each element of the claim. W.L. Gore & Associates v. Garlock, Inc., 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983), cert. denied 469 U.S. 851 (1984). Additionally, the single prior art reference must disclose each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221

U.S.P.Q. 481, 485 (Fed. Cir. 1984). "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention". Scripps Clinic & Research Foundation v. Genentech Inc., 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). "The identical invention must be shown in as complete detail as is contained in the ... claim". Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

The patent to Mehlhorn et al., does not disclose or suggest a circuit board having prefabricated borosilicate thin glass sheets having a thickness of less than or equal to 1.1 mm.

The patent to Mehlhorn et al. discloses a circuit carrier with integrated, active, optical functions which includes several layers of at least one insulating material and conductor structures located on or in the layers (see Abstract). The at least one optical layer is a polyimide layer (claim 9; col. 3, lines 46-47; col. 4 line 52). The optical layer can be constructed as a film or contained within a film (col. 5, lines 38-39).

According to the present invention, a high quality printed circuit board (PCB) with an optical conduction level can be manufactured with known PCB methods in a simple way by interconnecting at least one prefabricated thin glass sheet made of borosilicate glass of high optical quality and a carrier plate. Thin glass sheets made of borosilicate glass listed as examples used in the specification of the present

application, D 263 T and AF 45 by SCHOTT, are thin (30 micrometers to 1100 micrometers), flexible, have a superior flatness and extremely low surface roughness. They also have suitable thermal coefficients of expansion, have a high transmission in the visible and near infrared, and, unlike polyimide films, retain their shapes even at high temperatures. Some detailed product information regarding D 263 T and AF 45 thin glass sheets is attached to this amendment downloaded from the SCHOTT homepage www.schott.com.

Claims 1-2, 4-5, 7, 9-13, 15-17, 21 have also been rejected under 35 USC §102(b) as being anticipated by Tanahashi (JP-40-6167622A).

Tanahashi does not disclose or suggest a circuit board having prefabricated borosilicate thin glass sheets having a thickness of less than or equal to 1.1 mm.

According to the English abstract and the attached English computer translation of the application obtained from the Japanese PTO, Tanahashi teaches a circuit board and a method for manufacturing the circuit board. An electric wiring layer is embedded in a stack of quartz-glass layers which are formed one after another on a silicon substrate by a sol-gel process. According to par. [0006] of the application the purpose of the invention is to prepare an electric wiring layer in a quartz glass layer. as it is explained in par. [0015] of the description, the formation of each of the successive quartz-glass layers is done in a sol-gel process by spin coating the underlying sputtered conductor layer with a paste which is then heat treated at about 300 degrees. The

sputtering and spin coating processing methods are for in-situ preparing the glass layers. This is an expensive, more time consuming and complicated process. Unlike the present invention, the quartz-glass layers in Tanahashi are not prefabricated borosilicate thin glass sheets as recited in claims 1 and 15. Thus, claims 1 and 15 should be allowable.

Claims 2-14 depend from claim 1 and 16-21 depend from claim 15 should also be allowed.

Regarding claim 2, none of the cited prior art, either alone or in combination, disclose or suggest that the optical conduction level (OL) is formed by an optical sandwich (15; 15.1 ,..., 15.3) comprising, in addition to the minimum of one thin glass layer (11, 17), at least one carrier plate (10, 16) which is joined to the minimum of one thin glass layer (11, 17) over the area and including all the limitations of claim 1. Thus, claim 2 should be allowable.

Regarding claim 3, none of the cited prior art, either alone or in combination, disclose or suggest that the optical sandwich (15.1) comprises at least two carrier plates (10, 16) with a minimum of one thin glass layer (11) arranged between them and including all the limitations of claim 1. Thus, claim 3 should be allowable.

Regarding claim 4, none of the cited prior art, either alone or in combination, disclose or suggest that the optical sandwich (15.2, 15.3) comprises at least two thin glass layers (11, 17) which are joined over the area to the minimum of one carrier plate (10) and including all the limitations of claim 1. Thus, claim 4 should be allowable.

Regarding claim 5, none of the cited prior art, either alone or in combination, disclose or suggest that the minimum of two glass layer (11, 17) are joined together over the area and are arranged on one side of the minimum of one carrier plate (10) and including all the limitations of claim 1. Thus, claim 5 should be allowable.

Regarding claim 6, none of the cited prior art, either alone or in combination, disclose or suggest that the minimum of two glass layers (11, 17) are arranged on opposite sides of the minimum of one carrier plate (10) and including all the limitations of claim 1. Thus, claim 6 should be allowable.

Regarding claim 7, none of the cited prior art, either alone or in combination, disclose or suggest that the carrier plate (10, 16) are each made of an electrically insulating material which is used as the base material for the production of electric circuit boards and including all the limitations of claim 1. Thus, claim 7 should be allowable.

Regarding claim 8, none of the cited prior art, either alone or in combination, disclose or suggest that the carrier plates (10, 16) are each made of an Aramide reinforced resin and including all the limitations of claim 1. Thus, claim 8 should be allowable.

Regarding claim 9, none of the cited prior art, either alone or in combination, disclose or suggest that the thin glass layers (11, 17) and the carrier plates (10, 16) are glued or pressed together and including all the limitations of claim 1. Thus, claim 9 should be allowable.

(13) located in an optical conduction level (OL) are accessible from the outside through these coupling openings and including all the limitations of claim 1. Thus, claim 14 should be allowable.

Regarding claim 16, none of the cited prior art, either alone or in combination, disclose or suggest that the thin glass layer (11, 17) and the carrier plate (10, 16) are joined together by pressing or gluing and including all the limitations of claim 15. Thus, claim 16 should be allowable.

Regarding claim 17, none of the cited prior art, either alone or in combination, disclose or suggest that the thin glass layer (11, 17) joined to the carrier plate (10, 16) is structured between the first and second steps and including all the limitations of claim 15. Thus, claim 17 should be allowable.

Regarding claim 18, none of the cited prior art, either alone or in combination, disclose or suggest that the thin glass layer is removed in certain predetermined areas in order to structure the thin glass layer (11, 17) to form individual optical conductors (13) separated from one another by interspaces (12) and including all the limitations of claim 15. Thus, claim 18 should be allowable.

Regarding claim 19, none of the cited prior art, either alone or in combination, disclose or suggest that the removal of the thin glass layer (11, 17) is accomplished by means of lasers or by mechanical or chemical methods and including all the limitations of claim 15. Thus, claim 19 should be allowable.

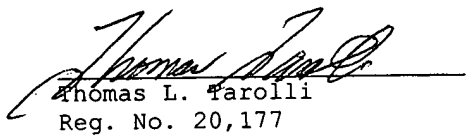
Regarding claim 20, none of the cited prior art, either alone or in combination, disclose or suggest that the free surface area of the structured thin glass layer (11) is coated with a reflective layer (29), preferably made of a metal, by vapour deposition, galvanic or chemical deposition and including all the limitations of claim 15. Thus, claim 20 should be allowable.

Regarding claim 21, none of the cited prior art, either alone or in combination, disclose or suggest that the interspaces (12) in the structured thin glass layer (11, 17) are filled with a filling material (14, 18) having a refractive index lower than the refractive index of the glass of the thin glass layer (11, 17) and including all the limitations of claim 15. Thus, claim 21 should be allowable.

In view of the foregoing, it is respectfully submitted that the above-identified application is in condition for allowance, and allowance of the above-identified application is respectfully requested.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,



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ENGLISCHE COMPUTERÜBERSETZUNG JP-406167622A

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]
[Industrial Application] this invention relates to the circuit board and its manufacture method, the circuit board for light-corpuscle children that a light-corpuscle child can carry especially, and its manufacture method.

[0002]
[Description of the Prior Art] The general circuit board for light-corpuscle children for carrying a light-corpuscle child mainly consists of electric wiring layers which are formed in the optical waveguide for being formed in the quartz-glass layer for being formed on a silicon substrate and a silicon substrate, and carrying a light-corpuscle child, and a quartz-glass layer, and performing transfer of a signal with a light-corpuscle child, and the front face of a quartz-glass layer, and consist of a conductive metal.

[0003] When manufacturing this kind of circuit board for light-corpuscle children, a quartz-glass layer is formed on a silicon substrate by the flame hydrolysis depositing method at a multilayer. Moreover, in parallel to the formation process of such a quartz-glass layer, an optical waveguide is formed between quartz-glass layers. An optical waveguide forms the quartz-glass layer which doped the germanium dioxide (GeO2) on a quartz-glass layer, and if it **********s to a predetermined pattern, it can form this quartz-glass layer. An electric wiring layer forms the thin film which consists of a conductive metal by the sputtering method etc. on the quartz-glass layer formed in the

multilayer, including an optical waveguide, and if it **********s to a predetermined pattern, it can form this thin film.

[0004]
[Problem(s) to be Solved by the Invention] Since the aforementioned conventional circuit board for light-corpuscle children has the electric wiring layer only on the front face of a quartz-glass layer, the densification of an electric wiring layer is difficult for it. Thus, since heat treatment of about 600 degrees C or more is needed when forming a quartz-glass layer by the flame hydrolysis depositing method and the electric wiring layer will oxidize at the time of above-mentioned heat treatment even if it is going to form an electric wiring layer between quartz-glass layers, the conventional circuit board for light-corpuscle children does not contain an electric wiring layer in a quartz-glass layer, because an electric wiring layer cannot be formed in a quartz-glass layer.

[0005] Therefore, since the conventional circuit board for light-corpuscle children cannot constitute a microstrip line for example, in a quartz-glass layer, it cannot transmit RF signals, such as microwave, to an electric wiring layer. The purpose of this invention is to prepare an electric wiring layer in a quartz-glass layer.

[0006]
[Means for Solving the Problem] The circuit board for light-corpuscle children concerning the 1st invention is the circuit board which a light-corpuscle child can carry. This circuit board is equipped with the electric wiring layer which is formed in a quartz-glass layer with the optical waveguide for being formed in the quartz-glass layer for being formed of a sol gel process on a silicon substrate and a silicon substrate, and carrying a light-corpuscle child, and a quartz-glass layer, and performing transfer of a signal with a light-corpuscle child, and consists of a conductive metal.

[0007] The manufacture method of the circuit board concerning the 2nd invention is the manufacture method of the circuit board for light-corpuscle children which a light-corpuscle child can carry. This method includes the following process.
O Process which forms a quartz-glass layer by the sol gel process on a silicon substrate at a multilayer.
O Process which forms the electric wiring layer which serves as an optical waveguide for

performing transfer of a signal with a light-corpuscle child from a conductive metal between quartz-glass layers in parallel to the process which forms a quartz-glass layer in a multilayer.

[0008]
[Function] In the circuit board for light-corpuscle children concerning the 1st invention, since it is formed of the sol gel process for which a quartz-glass layer does not need heat treatment by the elevated temperature, it has the electric wiring layer also in the quartz-glass layer. For this reason, in such the circuit board, the densification of the electric wiring layer can be carried out, for example in a quartz-glass layer.

[0009] By the manufacture method of the circuit board for light-corpuscle children concerning the 2nd invention, since the quartz-glass layer is formed in a multilayer by the sol gel process, in the formation process of a quartz-glass layer, elevated-temperature heat treatment like the flame hydrolysis depositing method becomes unnecessary. For this reason, since the conductive metal which constitutes an electric wiring layer cannot oxidize easily in the morphosis of a quartz-glass layer, it can form an electric wiring layer with an optical waveguide between quartz-glass layers. Consequently, according to this invention, the circuit board for light-corpuscle children equipped with the electric wiring layer in the quartz-glass layer can be manufactured.

[0010]
[Example] The circuit board for light-corpuscle children which starts one example of this invention at drawing 1 is shown. In drawing, the circuit board 1 for light-corpuscle children mainly consists of a silicon substrate 2 and a quartz-glass layer 3 formed on the silicon substrate 2. A silicon substrate 2 is the member of a tabular and has the 1st conductor layer 4 on the drawing upper surface. The 1st conductor layer 4 is the metallicity of aluminum, copper, etc.

[0011] Sequentially from the silicon-substrate 2 side, it is the layered product by which was reached, and the laminating of the 4th quartz-glass layer 8 was carried out to this order, and it was united with it 3rd quartz-glass layer 7, and the quartz-glass layer 3 is formed of the 1st quartz-glass layer 5, the 2nd quartz-glass layer 6, and the sol gel process that mentions each quartz-glass layers 5, 6, 7, and 8 later. Between the 1st quartz-glass

layer 5 and the 2nd quartz-glass layer 6, three tracks 9 prolonged in parallel mutually are formed in the direction which intersects perpendicularly with the space of drawing. Moreover, the 2nd conductor layer 10 is formed between the 2nd quartz-glass layer 6 and the 3rd quartz-glass layer 7. A track 9 and the 2nd conductor layer 10 all consist of conductive material, such as copper and aluminum, and constitute the strip line with the 1st conductor layer 4.

[0012] Moreover, between the 3rd quartz-glass layer 7 and the 4th quartz-glass layer 8, a series of optical waveguides 11 and internal wiring layers 12 are prepared. the signal with which a part of optical waveguide 11 was formed in the 4th quartz-glass layer 8 -- it has exposed with the hole 13 this signal -- the hole 13 is equipped with the micro prism which is not illustrated, and enables transfer of a lightwave signal between the optical waveguide 11 and the light-corpuscle child who mentions later In addition, an optical waveguide 11 consists of quartz glass with which a germanium dioxide and titanium oxide were doped by quartz glass. The internal wiring layer 12 is formed at the predetermined pattern configuration between the 3rd quartz-glass layer 7 and the 4th quartz-glass layer 8, and the part has connected it to the 2nd conductor layer 10. This internal wiring layer 12 also consists of conductive metals, such as copper and aluminum.

[0013] The front wiring layer 13 prepared in the predetermined pattern configuration and the loading section 14 are formed in the drawing upper surface of the 4th quartz-glass layer 8. the loading section 14 -- the drawing upper surface center section of the 4th quartz-glass layer 8 -- a signal -- it is prepared so that a hole 13 may be inserted, and the part has connected with the front wiring layer 13 Moreover, the loading section 14 has become depressed a little in the 4th quartz-glass layer 8 so that the light-corpuscle child 20 can be carried stably.

[0014] The light-corpuscle child 20 is carried in the loading section 14 of the above-mentioned circuit board 1 for light-corpuscle children. The light-corpuscle child 20 is being fixed to the loading section 14 by the solder bump 21 attached in it. Since such the circuit board 1 for light-corpuscle children has the internal wiring layer 12 also in the quartz-glass layer 3 in addition to the front wiring layer 13, it can carry out densification of the electric wiring layer compared with the conventional circuit board for light-corpuscle children. Moreover, since the strip line is formed in the quartz-glass layer 3, RF signals,

such as microwave, can be transmitted. Furthermore, since the dielectric constant is small, the quartz-glass layer 3 has the small propagation delay of a signal in internal wiring layer 12 grade. Moreover, since the dielectric dissipation factor (tandelta) is small, in the strip line, loss of microwave is small.

[0015] Next, the manufacture method of the aforementioned circuit board 1 for light-corpuscle children is explained. First, as shown in drawing 2 , a silicon substrate 2 is prepared. As shown in drawing 3 , the 1st conductor layer 4 is formed in the drawing upper surface of this silicon substrate 2. The 1st conductor layer 4 can be formed by film methods, such as the sputtering method. Next, as shown in drawing 4 , the 1st quartz-glass layer 5 is formed on the 1st conductor layer 4. The 1st quartz-glass layer 5 is formed by the sol gel process. A sol gel process makes the solution (sol) of a metaled organic compound or an inorganic compound gel by the hydrolysis and the polycondensation reaction between compounds, and means the method of obtaining the solid-state of an oxide, by heating this gel. When forming the 1st quartz-glass layer 5 by such sol gel process, Si(OC2H5)4 280g, 1440ml (H2 O) of water, ethanol (C2 H5 OH) 79ml, and the paste containing 0.3ml (HCl) of hydrochloric acids are uniformly applied on the 1st conductor layer 4 by the paste viscosity of 2.0cps, and the spin coat method of the conditions for 1000rpm / 10 seconds. And if this is heat-treated at about 300 degrees C, the 1st quartz-glass layer 5 will be formed on the 1st conductor layer 4. The morphosis of the quartz glass from an above-mentioned paste is shown by the following reaction formula.

[0016]
[Formula 1]

Next, as shown in drawing 5 , on the 1st quartz-glass layer 5, a film method is used and the metal thin film layers 22, such as aluminum, are formed. Then, as the Fort Lee

SOGURAFU method is adopted and this metal thin film layer 22 is shown in drawing 6 , it **********s. Thereby, a track 9 is formed on the 1st quartz-glass layer 5.

[0017] Next, as shown in drawing 7 , on the 1st quartz-glass layer 5 in which the track 9 was formed, an above-mentioned sol gel process is adopted, the 2nd quartz-glass layer 6 is formed, and the 2nd conductor layer 10 is further formed by the film method on the 2nd quartz-glass layer 6. Moreover, on the 2nd conductor layer 10, as shown in drawing 8 , the 3rd quartz-glass layer 7 is formed by the same sol gel process. Next, as shown in drawing 9 , a through hole 23 is formed in the predetermined part of the 3rd quartz-glass layer 7. This through hole 23 is for forming the internal wiring layer 12, for example, if reactive ion etching is given to the 3rd quartz-glass layer 7 using a positive resist, it can be formed.

[0018] Thus, as shown in the 3rd quartz-glass layer 7 in which the through hole 23 was formed at drawing 10 , the internal wiring layer 12 is formed in the side and the base of the through hole 23 near the through hole 23 by the film method. As shown in drawing 11 after formation of the internal wiring layer 12, the quartz-glass layer 24 by which a germanium dioxide and titanium oxide were doped is formed on the 3rd quartz-glass layer 7. It sets to an above-mentioned sol gel process, and such a quartz-glass layer 24 is Si (OC two H5)4. It is germanium (OC two H5)4 about a part. Ti4 (OC two H5) It can form, if it replaces.

[0019] Next, reactive-ion-etching processing is performed to a predetermined pattern configuration to the quartz-glass layer 24. Thereby, as shown in drawing 12 , an optical waveguide 11 is formed on the 3rd quartz-glass layer 7. Next, as shown in drawing 13 , the 4th quartz-glass layer 8 is formed by the above-mentioned sol gel process on the 3rd quartz-glass layer 7 in which the optical waveguide 11 was formed. and the crevice 25 for forming the loading section 14 in the predetermined part of the 4th quartz-glass layer 8, as shown in drawing 14 and a signal -- a hole 13 is formed by the reactive-ion-etching method the [and] -- by adopting a film method and the etching method to 4 quartz-glass layers 8, as shown in drawing 15 , the front wiring layer 13 and the loading section 14 are formed Thereby, the circuit board 1 for light-corpuscle children is obtained.

[0020] Since the quartz-glass layer 3 is formed by the sol gel process, high temperature processing like [in the case of forming a quartz-glass layer by the flame hydrolysis depositing method] is not required of the manufacturing process of the above circuit

boards 1 for light-corpuscle children. Therefore, in the formation process of the quartz-glass layer 3, since the 1st conductor layer 4, a track 9, the 2nd conductor layer 10, and the internal wiring layer 12 do not oxidize, these electric wiring layers can be formed in the quartz-glass layer 3.

[0021]

[Effect of the Invention] According to the 1st and 2nd invention, since the quartz-glass layer is formed on a silicon substrate by the sol gel process, the circuit board for light-corpuscle children containing the electric wiring layer which consists of a conductive metal in a quartz-glass layer can be offered.

CLAIMS

[Claim(s)]

[Claim 1] The circuit board for light-corpuscle children which is the circuit board for light-corpuscle children a light-corpuscle child can carry the circuit board, and equipped with a silicon substrate, the quartz-glass layer for carrying an aforementioned light-corpuscle child a layer was formed in an aforementioned silicon-substrate top of a sol gel process, the aforementioned light-corpuscle child and the optical waveguide for [of a signal] delivering and receiving an optical waveguide was formed in an aforementioned quartz-glass layer, and the electric-wiring layer which consist of the conductive metal a metal was formed in an aforementioned quartz-glass layer.

[Claim 2] The manufacture method of the circuit board for light-corpuscle children which is the manufacture method of the circuit board for light-corpuscle children which a light-corpuscle child can carry, and includes the process which forms the electric wiring layer which serves as an optical waveguide for performing transfer of a signal with the aforementioned light-corpuscle child from a conductive metal between the aforementioned quartz-glass layers in parallel to the process which forms a quartz-glass layer by the sol gel process on a silicon substrate at a multilayer, and the aforementioned process.

[Translation done.]

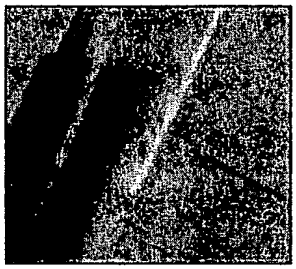
Thin Glass From SCHOTT - only 'nothing' is less

0.030 mm thin

Supporting consumer needs for thinner, lighter and flatter products SCHOTT Displayglas produces the thinnest glass in the world with only 0.030 mm - that is where the glass substrate is nothing at all.

Flexible

Like a foil, thin glass can be matched up to a bending radius to a certain degree. In this way, thin glass can be incorporated into complicated structures.

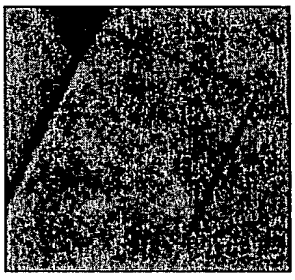


Superior flatness

Minimum deviations in flatness and thickness along with an extremely low surface roughness provide you with the optimum substrate for your product.

Matching CTEs

The thermal coefficients of expansion of D 263 T and AF 45 are in line with the coating types used in the electronics industry.

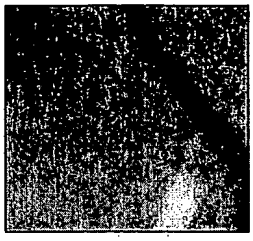


Chemically resistant

No matter whether you structure your coatings with acid, alkali or water, D 263 T and AF 45 are resistant to these attacks.

Transmission

Both D 263 T and AF 45 have a high transmission in the visible and near infrared range.

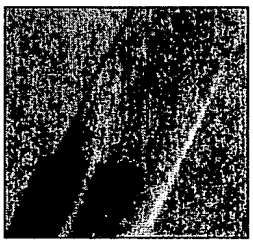


Thermally resistant

Your production requires high processing temperatures? D 263 T and AF 45 borosilicate substrates retain their shapes, even at high temperatures.

Dimensions

Different products need different substrates. That is why we are not only offering standard sized sheets but also sizes according to your specific requests - small as well as large sizes.



Highest quality standards

Our process is subject to strictest quality management standards to ensure that substrates of a constant high quality level. Continuous process optimization plus process control and permanent quality monitoring are part of this system.

Products **D 263 T**

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D 263 T is a borosilicate glass which is produced by melting the purest raw mate

- Main characteristics
- Thermal Properties
- Mechanical Properties
- Chemical Properties
- Electrical Properties
- Optical Properties

The main characteristics of this glass type are:

- Low alkali content
- Highly resistant to chemical attack
- High luminous transmittance
- Easy to cut
- Excellent flatness
- Fire polished surfaces

Dimensions

- Maximum dimensions: 440 mm x 360 mm (larger upon request)
- Thickness: 30 µm to 1100 µm (special thicknesses upon request)

Edge Working

- Bevelled edges or cut edges, seamed
- Corner cut

Options

- Dimensions, processing steps and tolerances according to customer specif
- Square substrates in all thicknesses, round/wafer form from 150 µm thick upwards
- Compaction treatment

in keeping with the latest technical standards.

Thermal Properties

Viscosity and Corresponding Temperature

Designation	Viscosity log η [dPas]
Strain Point	14.5
Annealing Point	13.0
Softening Point	7.6

Transformation Temperature T_g in °C

Coefficient of Thermal Expansion α

Coefficient of Mean Linear Thermal Expansion $\alpha_{(20\text{-}300°C)}$ in $10^{-6}\ K^{-1}$ (Static Measurement)

Mechanical Properties

Density ρ in g/cm^3 (annealed at 40°C/h)	2.51
Stress Optical Coefficient C in $1.02 \cdot 10^{-12}\ m^2/N$	3.4
Young´s Modulus E in kN/mm^2	72.9
Poisson´s Ratio μ	0.208
Torsion Modulus G in kN/mm^2	30.1
Knoop Hardness HK_{100}	590

Chemical Properties

Hydrolytic Resistance acc. to DIN ISO 719

Hydrolytic Class	HGB 1
Equivalent of Alkali (Na_2O) per gram of glass grains in μg/g	20

Acid Resistance acc. to DIN 12116

Acid Class	2
Half Surface Weight Loss after 6 hours in mg/dm^2	1.4

Alkali Resistance acc. to DIN ISO 695

Class	A 2
Surface Weight Loss after 3 hours in mg/dm^2	88

Electrical Properties

Dielectric Constant (Permittivity) ε_r at 1 MHz	6.7
Dissipation Factor tan δ at 1 MHz	$61 \cdot 10^{-4}$

Electric Volume Resistivity ρ_D in Ω · cm at the Specified Temperatures ρ_D for Alternati Hz

θ = 250 °C	
θ = 350 °C	

Optical Pr perties

Refractive Indices

Pretreatment of Samples	n_g	**1.5354**
Condition as supplied [´as drawn´]	$n_{F'}$	**1.5305**
	n_F	**1.5300**
	n_e	**1.5255 +/- 0.0015**
	n_d	**1.5231**
	n_D	**1.5230**
	$n_{C'}$	**1.5209**
	n_C	**1.5204**
Abbé Value	v_e	**55**

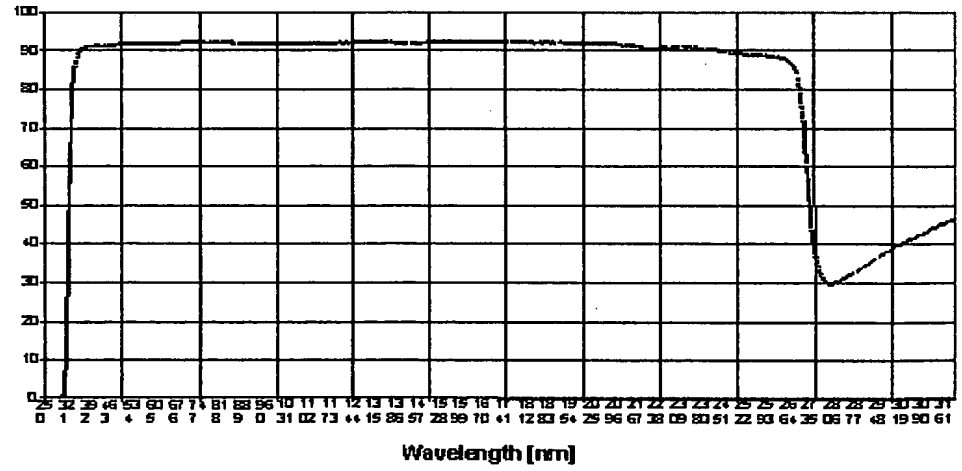
Transmittance Data τ_λ - Individual Values in % (t = 1.1 mm)

λ [nm]	τ_λ [%]
380	89.8
632.8	91.8
1064	92.0

Edge Wavelength (t=1.1 mm)

Edge Wavelength λ_C (τ = 0.46) in nm	**329**
Luminous Transmittance τ_{vD65} in % (t=1.1 mm)	**91.2**
t = 1.1 mm	**91.7 ± 0.3**

Spectral Transmittance of D 263 T, t=1.1



Products **AF 45**

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AF 45 is a modified borosilicate glass with a high content of BaO and Al_2O_3. I synthesis.

- Main characteristics
- Thermal Properties
- Mechanical Properties
- Chemical Properties
- Electrical Properties
- Optical Properties

Main characteristics of this glass type are:

- Alkali free
- Low coefficient of expansion
- Excellent thermal resistance
- High luminous transmittance
- Excellent flatness
- Fire polished surfaces

Dimensions

- Maximum dimensions: 440 mm x 360 mm (larger upon request)
- Thickness: 50 µm to 1100 µm (special thicknesses upon request)

Edge Working

- Bevelled edges or cut edges, seamed
- Corner cut

Options

- Dimensions, processing steps and tolerances according to customer sp
- Square substrates in all thicknesses, round / wafer form from thickness upwards
- Compaction treatment

standards and measuring methods. SCHOTT Displayglas retains the right to c
in keeping with the latest technical standards.

Thermal Properties

Viscosity and Corresponding Temperature

Designation	Viscosity log η [dPas]
Strain Point	14.5
Annealing Point	13.0
Softening Point	7.6

Transformation Temperature T_g in °C

Coefficient of Termal Expansion α

Coefficient of Mean Linear Thermal Expansion $\alpha_{(20\text{-}300°C)}$ in 10^{-6} K^{-1} (Static Measurement)

Mechanical Properties

Density ρ in g/cm^3 (annealed at 40°C/h)	2.72
Stress Optical Coefficient C in $1.02 \cdot 10^{-12}$ m^2/N	3.2
Young´s Modulus E in kN/mm^2	66.0
Poisson´s Ratio μ	0.235
Torsion Modulus G in kN/mm^2	26.7
Knoop Hardness HK_{100}	555

Chemical Properties

Hydrolytic Resistance acc. to DIN ISO 719

Hydrolytic Class	HGB 1
Equivalent of Alkali (Na_2O) per gram of glass grains in μg/g	6.8

Acid Resistance acc. to DIN 12116

Acid Class	4
Half Surface Weight Loss after 6 hours in mg/dm^2	> 250

Alkali Resistance acc. to DIN ISO 695

Class	A 3
Surface Weight Loss after 3 hours in mg/dm^2	460

Electrical Properties

Dielectric Constant (Permittivity) ε_r at 1 MHz	6.2
Dissipation Factor tan δ at 1 MHz	$9 \cdot 10^{-4}$

Electric Volume Resistivity ρ_D in Ω · cm at the Specified Temperatures ρ_D for Direc

θ = 250 °C

	$6.0 \cdot 10$
θ = 350 °C	$3.2 \cdot 10^{1}$
θ = 500°C	$1.6 \cdot 10^{5}$

Temperature t_{k100} in °C for a Specific Electric Volume Resistivity of 10^8 Ω · cm	610

Optical Properties

Refractive Indices		
Pretreatment of Samples	n_g	1.5359
Condition as supplied [´as drawn´]	$n_{F'}$	1.5318
	n_F	1.5313
	n_e	1.5275
	n_d	1.5255
	n_D	1.5254
	$n_{C'}$	1.5233
	n_C	1.5229
Abbé Value	v_e	62.2

Transmittance Data Edge Wavelength (t = 1.1 mm)	
Edge Wavelength λ_C (τ=0.46) in nm	315
Luminous Transmittance τ_{vD65} in % (t=1.1 mm)	91.2